Design Task 2:
Single Stage 2N2222A Amplifier

ES21J Analogue Design

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Abstract

The aim of this laboratory was to design and test a single stage amplifier using a 2N2222A Transistor. An amplifier was designed theoretically and its behaviour tested using PSPICE. When a satisfactory design was produced it was assembled on a breadboard. This was then tested to confirm the predicted operation. Graphs of Gain, Phase, Z_O and Z_I were produced for the simulation and practical evaluation. The operation was found to be a good approximation to that predicted in the simulation with the same gain being produced in the mid-band and approximately the same lower cut off point. The upper cut off point was found to be lower than predicted but the variance in this can be accounted for by the varying high frequency response of each device. Generally the gain an phase corresponded with the simulated and predicted values. It was found that although it was easy to create a simulated model that produced the required behaviour in practice many non-simulated factors affected the results produced. This proves the importance of prototyping even with more complex simulators.

Introduction

A single stage amplifier based on the 2N2222A transistor and the specification below is to be designed and tested using a simulation tool (PSPICE). A design will initially be produced theoretically on paper. The design will then be simulated using PSPICE, a powerful electronic simulation tool. When the simulated design is shown to confirm to the specification the design will be produced on a breadboard and tested. Graphs of Gain, Phase, Z_O and Z_I will be produced for the simulation and practical evaluation. The results from the practical evaluation will be compared to the results predicted from the simulation.

Specification

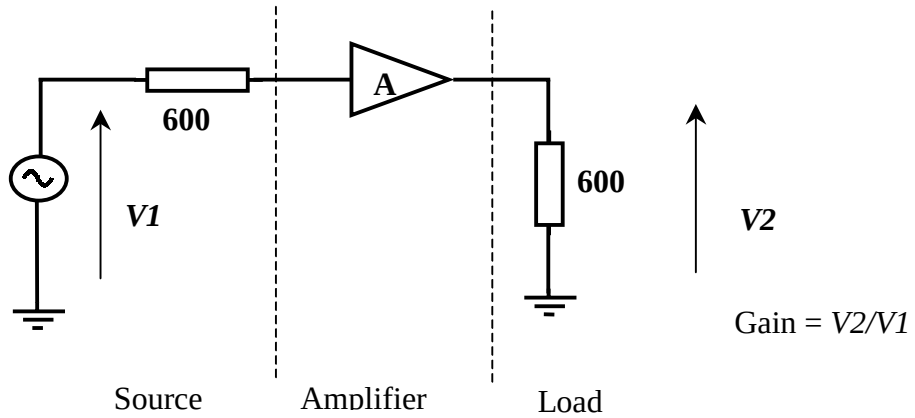
Design a single-stage amplifier, using a 2N2222A transistor, to the following specification.

Internal resistance of ac signal source = 600 Ω

dc supply voltage – 12V

dc current not to exceed 15 mA

Voltage gain – at least 20 dB at mid-band into a 600 Ω load



Frequency Response

Lower cut-off frequency of 40 Hz

Higher cut-off frequency of 4 MHz

(All for fixed input voltage)

Power Output

Level at which clipping starts to be not less than 2.0 mW rms. in a 600 Ω load at mid-band.

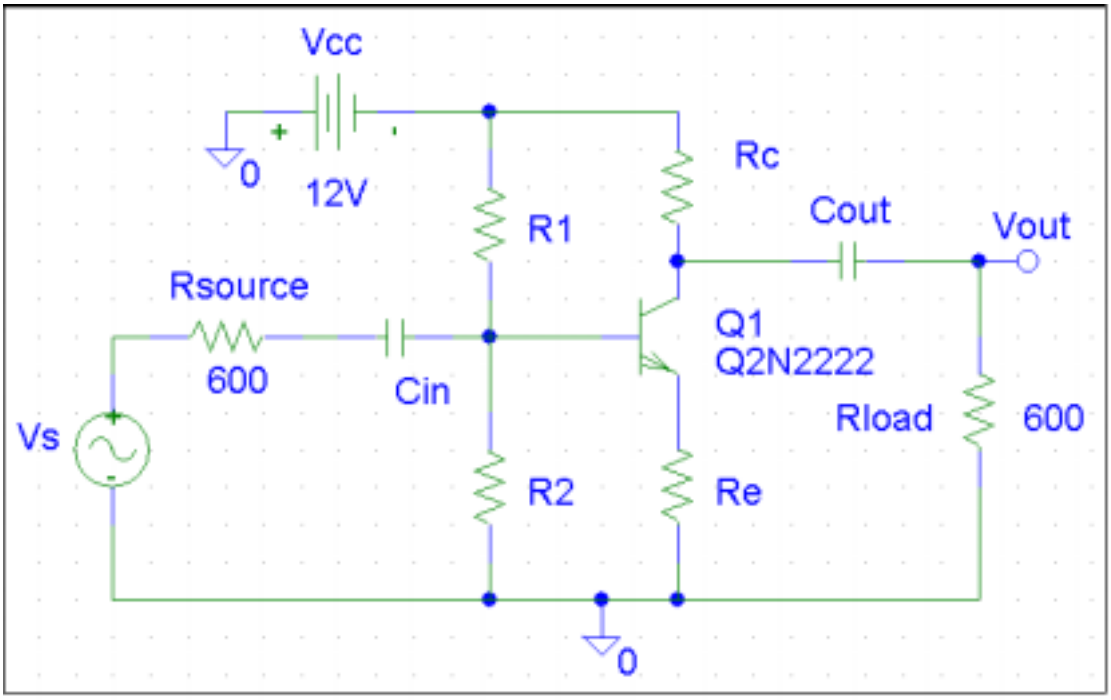
Input and Output Impedance

$|Z_{in}|$ to be within limits 600 Ω ± 10% at mid-band

$|Z_{out}|$ to be within limits 600 Ω ± 10% at mid-band

Theoretical Design

The first thing to consider is the type of configuration required to produce the required operating characteristics in the specification. From a comparison of the various characteristics if can be seen that a common emitter is the most viable since this is the only configuration that can provide the high voltage and current gain required.
Taking into account the specification, (input voltage, load resistance etc.) the circuit below is therefore required (Load is 600Ω to maximise power transfer):



Since output impedance = $\frac{1}{h_{oe}} \| R_c$ and $\frac{1}{h_{oe}}$ is very large it can be assumed that output impedance = R_C and therefore R_C = 600Ω. To maintain thermal stability V_{RE} should be 20-30% of $V_{CC.}$ V_{CC} = 12V so a V_{RE} of 3V is chosen.

$$R_E = R = \frac{V_{RE}}{I_C} = \frac{3}{10x10^{-3}} = 300\Omega$$

Therefore a value of 300Ω is chosen for R_E.

V_{BB} must now be calculated.

$$V_{BB} = V_{RE} + 0.7$$

$V_{BB} = 3.7V$

$R_B = R_1 || R_2$

$$\frac{1}{R_B} = \frac{1}{R_1} + \frac{1}{R_2}$$

and:

$$V_{BB} = \frac{R_2}{R_1 + R_2} \times V_{CE}$$

Therefore:

$$\frac{1}{600} = \frac{1}{R_1} + \frac{1}{R_2} \qquad 3.7 = \frac{12R_2}{R_1 + R_2}$$

Solve:

$$R_1 = 2.25R_2$$

$$\therefore \frac{1}{600} = \frac{1}{2.25R_2} + \frac{1}{R_2}$$

$$R_2 = 870\Omega \; R_1 = 1950\Omega$$

This should give a Q point around 6V therefore allowing a reasonable input voltage to be used.
However the values will have to be adjusted slightly since they are not preferred values.

In order to achieve the 40Hz lower cut-off the coupling capacitor value was calculated as shown below:

$$f_{CO} = \frac{1}{2\pi RC} = 6.6\text{uF}$$

In order to achieve the 4MHz upper cut-off the base-emitter must be bypassed at high frequencies. A capacitor is used to do this, its value was calculated as shown below:

h_{ie} = 0.25Ω - 1.25kΩ = 0.75kΩ = 750Ω (See data sheet in appendix)

Note: There is a variation in h_{ie} between devices, only an approximation is used. This may affect the upper cut-off frequency.

Upper cut-off frequency:

$$h_{ie} = \frac{1}{2\pi fC} = \frac{1}{2\pi(4x10^6)C}$$

c ≈ 53pF (across BE)

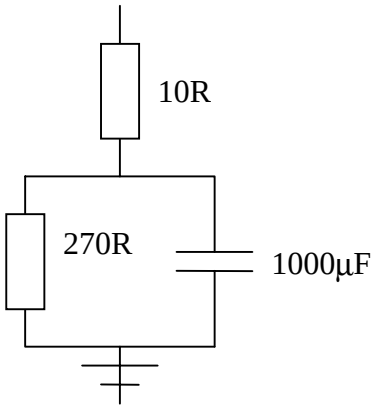
A gain of at least 10 (20dB) is required. To do this a portion of R_E must be made to pass AC but stop DC (thereby maintaining the bias point). The value of R_E was split into two, R_{E1} and R_{E2}, For a high gain most of R_E would need to be bypassed by AC. Therefore R_{E1} had to be much smaller than the R_{E2}. A capacitor is used to allow the

AC to pass. This must pass all frequencies used (40Hz – 4MHz). It must not attenuate frequencies required to any relevant degree. Therefore a cut-off considerably less than the lower cut-off frequency of 40Hz is required so that no attenuation occurs. Therefore:

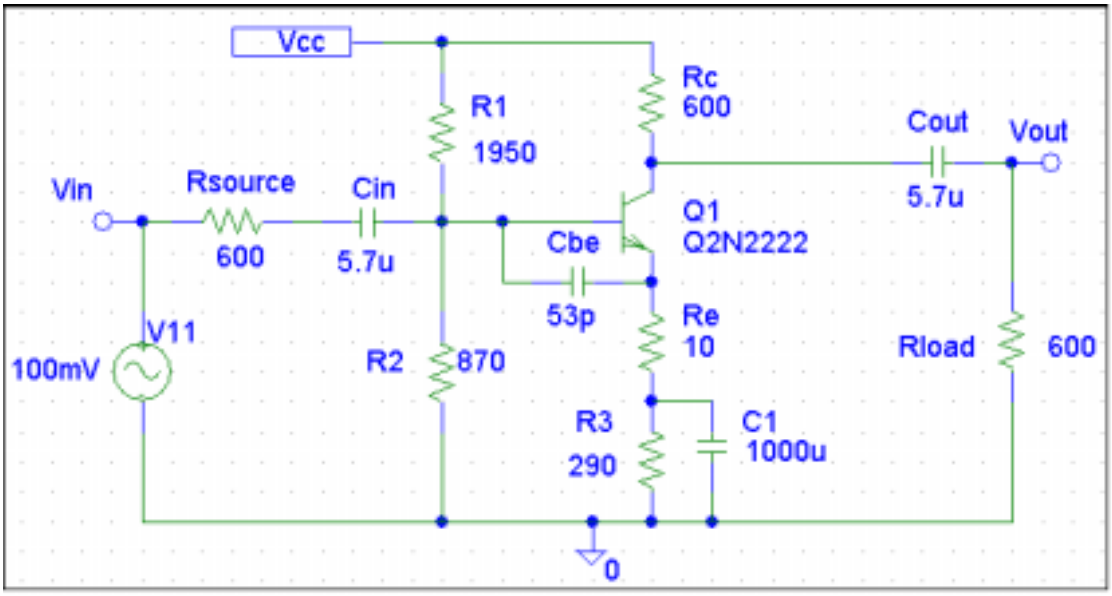
$$f_{CO} = \frac{1}{2\pi RC}$$

$$C \approx 1000\mu F$$

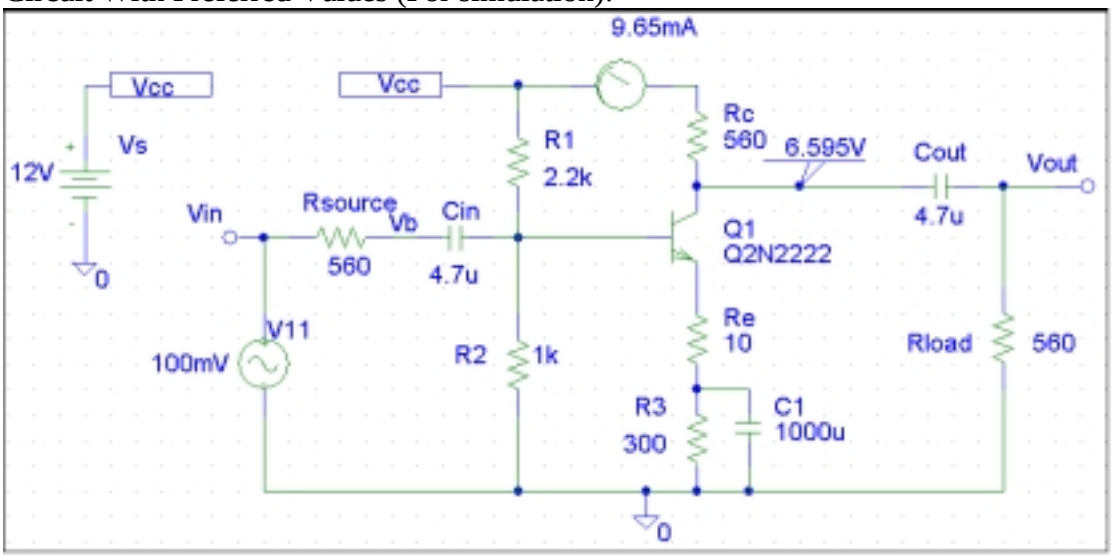
The arrangement opposite gives about a 20dB mid band gain as required



Final Circuit:



Circuit With Preferred Values (For simulation):



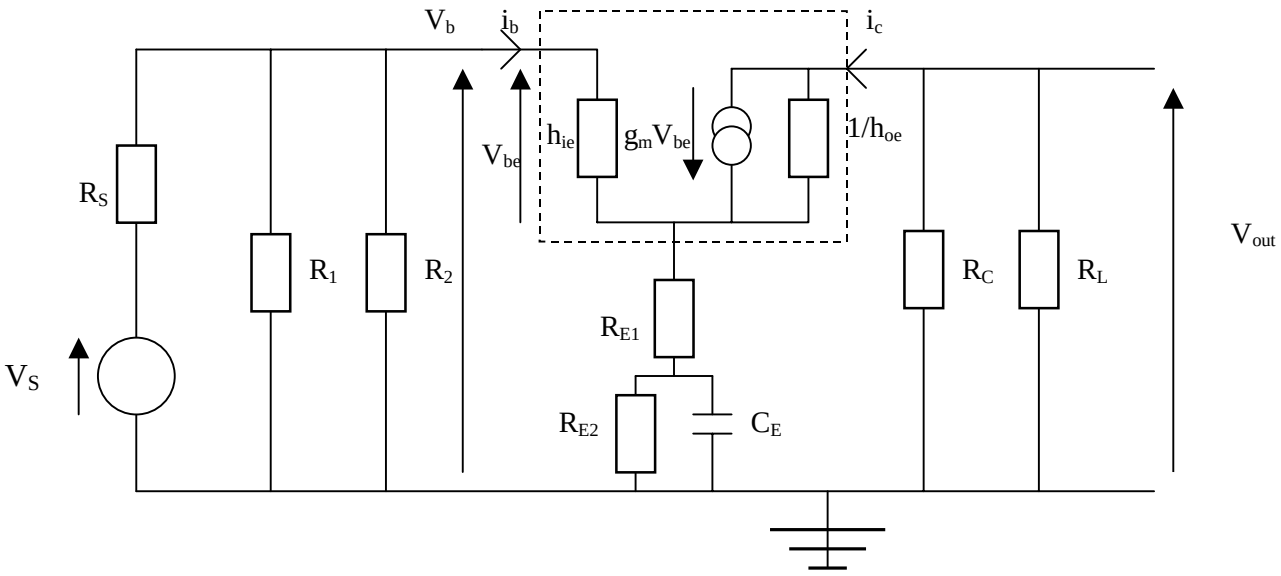
The preferred values may change to results from those predicted slightly but this variation should be minimal.

Calculation of Z_{in} and Z_{out}.

$Z_{out} = 1/h_{oe} \parallel R_C$
According to data sheet (See Appendix A):
h_{oe} = 15-200μohms
Therefore: $Z_{out} \approx 600\Omega$.

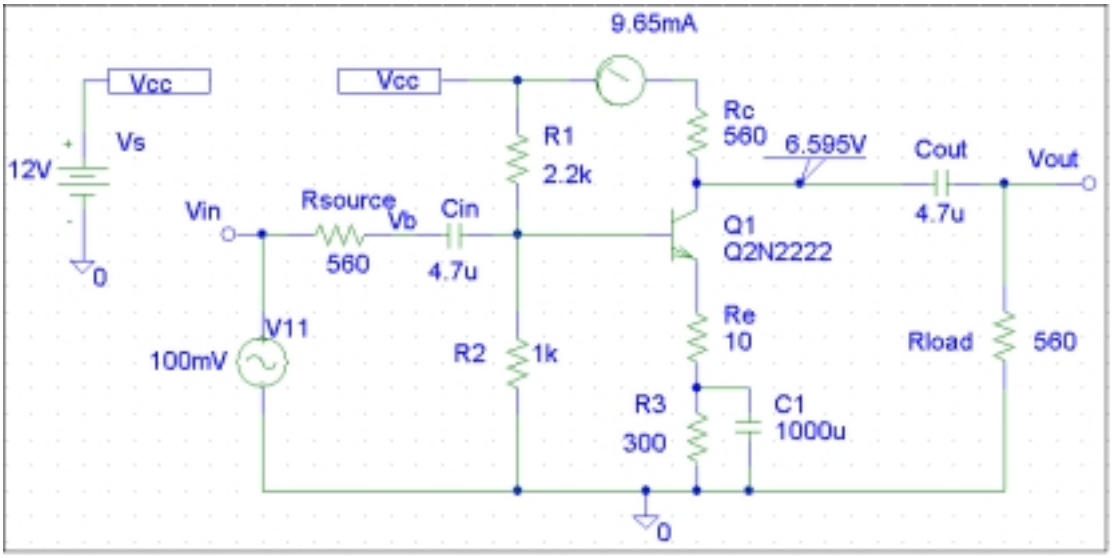
$Z_{in} = h_{ie} // R_B$
$R_B = R_1 \parallel R_2$
h_{ie} is large compared to R_B (See data sheet, Appendix A). So:
$Z_{in} \approx R_B$
Rb ≈ 600Ω

Equivalent Circuit:



Simulation

The circuit was drawn in Microsim schematics (as shown below) and simulated using PSPICE.

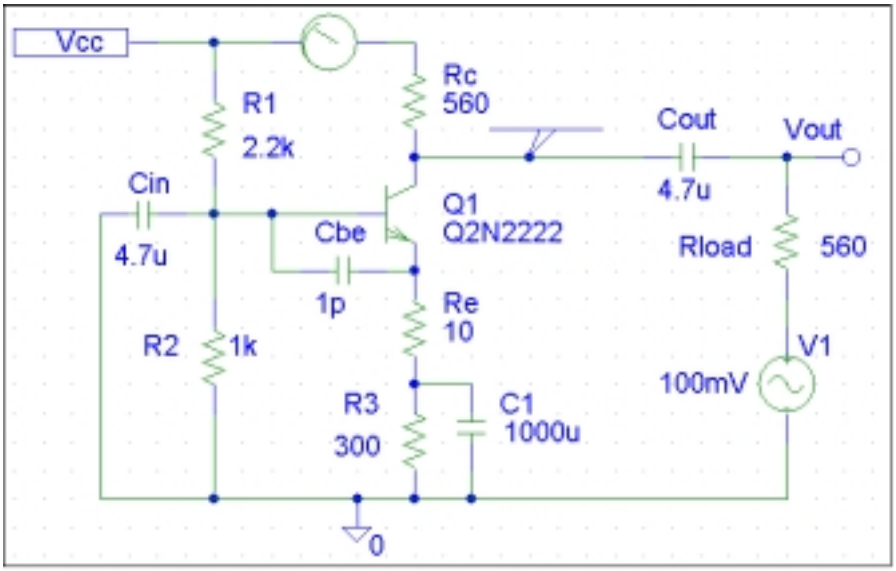


The netlist is shown below:

```
** amp1.net **
V_Vs          Vcc 0 12V
C_C1          0 1  1000u
V_V11         Vin 0 DC 0V AC 100mV
R_Rsource     Vin Vb  560
R_Rload       0 Vout  560
R_R3          0 1  300
R_Rc          3 2  560
C_Cin         4 Vb  4.7u
C_Cout        2 Vout  4.7u
R_R1          Vcc 4  2.2k
R_R2          4 0  1k
Q_Q1          2 4 5 Q2N2222
R_Re          5 1  10
v_V5          Vcc 3 0
```

Graphs of the gain, phase, Zi and Zo against frequency were produced.
All the measurments used an AC sweep from 10Hz to 10MHz using a 100mV sinusoidal (AC) source. Gain and phase were ploted using inbuilt functions (See graphs).

Z_i was measured by taking the voltage at V_b and the current through R_{source}. $\frac{V_b}{R_{source}} = Z_i$. The circuit was altered slightly to measure Z_o. Point V_b was grounded and a the source was placed after R_{load} as shown below:



AC analysis was run and Zo was calculated as follows: $\frac{V_{out}}{R_{load}} = Z_o$.

Some component values predicted were changes as a result of the simulation to give better results.

The graphs produced (Gain, Phase Zi, Zo) are shown on the next 4 pages:

Using the probe it can be seen there is a lower cut-off around 40Hz and an upper cutoff at about 4MHz (See Graph).
The mid-band gain is just above 20dB as required.
The phase gives about –180º in the mid band as required.
Both Z_I and Z_O are about 600Ω in the mid-band as required.
The results from the simulation confirm to the specification, suggesting the amplifier will perform as required.

Practical Evaluation

The circuit, as shown previously, was assembled on a breadboard for practical evaluation. A signal generator was used for the input. The input voltage used was 100mV (As in simulation). A conventional oscilloscope was used to take the measurements. The oscilloscope cannot provide the accuracy of more specialist instruments (e.g. an electronic oscilloscope) but is suitable for this investigation as high accuracy is desirable, not required. One input to the oscilloscope was connected to the input (sine wave oscillator) and one to the output. By adjusting the scales and using simple calculations the gain was measured at intervals from 10Hz to 10MHz. The phase was also measured over the same range. This was done on the oscillator by calculating the time lag relative to the period of the input and output. The input was found to lead the output.

The input and output impedances were determined in the same way as during the simulation. The current however was measured using an ammeter which measured the r.m.s current. This was converted to the peak current before the calculations were performed.

The lower/upper cut-offs (-3dB off mid-band gain) were determined by measuring the frequencies at a gain of 7.08. The lower cut-off was found to be to be 50Hz and the upper cut-off was found to be 1.6MHz. The lower cut-off variance is probably due to the variation in component value for the coupling capacitor which had to be changed due to availability. A better approximation to the desired frequency could probably be obtained by combining capacitors to get to desired value but component tolerances mean this is only of limited use. The upper cut-off is probably due to the transistors own internal base-emitter capacitance no base-emitter bypass transistor was used in the simulation so the simulated transistors own base-emitter capacitance caused the cut-off to be 4MHz. If the actual capacitor being investigated had a higher base-emitter capacitance (as seems the case) the upper cut-off would be lower as observed. The capacitance is known to vary considerably for each device.

The mid-band input impedance was found to be about right at about 640Ω however the output mid-band impedance was considerably higher than 600Ω at nearly 2kΩ. Also an increase in impedance was found at higher frequencies that was not predicted in the simulation. This again could be due to the capacitors high frequency characteristics. The input impedance was unmeasurable at higher frequencies since the current was too low to register on the ammeter used.
The data recorded is shown below:

Frequency (Hz)	Gain	Phase (º)
10	0.63	0.0
20	2.50	-43.2
30	4.00	-64.8
40	5.00	-86.4
50	6.25	-108.0
60	6.75	-129.6
70	7.25	-131.0
80	7.70	-132.2
100	8.25	-140.4
150	8.75	-156.6
300	9.50	-166.6
500	9.75	-171.0
5000	9.75	-180.0
50000	9.75	-180.0
100000	9.41	-180.0
500000	8.75	-202.5
800000	8.13	-209.3
1000000	7.75	-216.0
1200000	7.25	-225.0
1400000	6.75	-234.0
1600000	6.25	-243.0
2000000	5.63	-248.0
3000000	4.25	-252.0
4000000	3.25	-259.2
5000000	2.63	-266.0
10000000	1.10	-288.0

Frequency	Zi (Ω)	Zo (Ω)
10	11000	703
20	2556	604
40	1990	589
60	1898	578
80	1830	589
100	1832	578
500	1768	594
5000	2036	945
50000	4821	1343
100000	#N/A	1414
200000	#N/A	2874
300000	#N/A	88400
500000	#N/A	187900
800000	#N/A	150200
1000000	#N/A	157000
1200000	#N/A	139000
1400000	#N/A	125000
1600000	#N/A	113000
2000000	#N/A	104000
4000000	#N/A	54400
6000000	#N/A	39100
10000000	#N/A	18800

The graphs produced (Gain, Phase Zi, Zo) are shown on the next 4 pages:

Further Discussion/Conclusion

The specified operation, simulated operation and practical operation of the amplifier differed, but not considerably. The theoretical calculations provided a very close approximation to the specification. Using PSPICE the amplifier was made to almost exactly match the specification. However in practice many other factors altered the actual results. Higher precision components would have helped with the lower cut-off frequency as this is easily changed. The upper cut off however was influenced greatly by the internal parameters of the transistor, affecting its high frequency behaviour. From the graphs it can be seen that the gain is nearly as predicted at 20dB. The simulated and practical phase graphs are also similar, the method of calculating the phase used in the practical evaluation was inaccurate and therefore there may be a considerable error in the phase measurements. This is demonstrated by a less than smooth line. An electronic oscilloscope or other phase measuring tool would have been a considerable more accurate (and indeed quicker) way of measuring the phase.
The input impedance was generally satisfactory. Apart from the low currents preventing measurements at higher frequencies it can be concluded that the mid-band input impedance it within the limits (600 Ω ± 10%) given in the specification. The mid band output impedance was around 1800-1900 and so was unsatisfactory. This is surprising since the simulation predicted the correct value. It is therefore possible that this was measured wrong and a re-evaluation of the results would be a good idea. The design could be improved be altering the design to take account of the high frequency behaviour. Also extra stages could be added, giving more flexibility and therefore possible a more stable design. Overall it was found that although it was easy to create a simulated model that produced the required behaviour in practice many non-simulated factors affected the results produced. This proves the importance of prototyping even with more complex simulators becoming available.

Bibliography

- Lecture Notes - ES21J Analogue Design
- Assignment Sheet - ES21J Analogue Design
- N. Storey, *Electronics: A Systems Approach,* Prentice Hall.

Appendix A: Transistor Data Sheet

Appendix B: Additional Printouts